Chip-scale Integrated Driver for Electrostatic DM Control

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1. Introduction

A complementary metal oxide semiconductor (CMOS) electronics driver chip to control a microelectromechanical (MEMS) deformable mirror (DM) has been developed. MEMS DMs have a wide range of uses in correcting time-varying aberrations in microscope and telescope imaging, laser beam forming applications and secure free-space communications. MEMS DMs that have been demonstrated are often quite small and consume very little power. Correspondingly, small electronic drivers would allow adaptive optics systems of unprecedented compactness.

With the advances in CMOS technology, it has become possible to design and fabricate electronics operable at higher voltages than those in traditional integrated circuits. Since MEMS structures often require relatively high operating voltages to energize electrostatic actuators, these high voltage CMOS fabrication processes offer promise for miniaturization of the corresponding drivers.

This paper introduces an integrated electronic driver developed to operate one particular type of MEMS mirror structure, requiring more than a hundred independently addressable control channels, each of which can be varied from ground potential to hundreds of volts.

2. Motivation

The purpose of this work was to design, simulate, fabricate and test a high voltage chip level driver to control a deformable MEMS mirror array. The MEMS mirror structure consists of 144 parallel-plate electrostatic actuators distributed beneath a continuous membrane deformable mirror.

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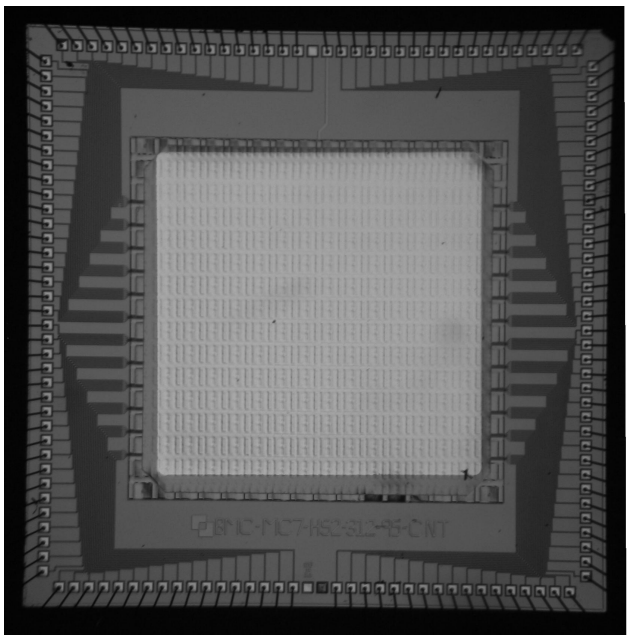

Figure 1 - 144 channel MEMS mirror

Figure 1 is a microphotograph of the DM, centered on a chip measuring 10mm on a side. Each of the 144 electrodes is can be controlled with an analog input measureing from 0V to 300V. At 300V, the actuator would impose a local deflection on the mirrorof about 4μm. Currently, the driver for this MEMS DM consists of an assembly of discrete electronic components mounted in metal chassis measuring 0.5m x 0.3m x 0.1m. If the CMOS version of the driver meets with success, it will reduce the size of that driver to the same scale as that of the DM itself. Such a compact system might find uses in applications requiring compactness and low power, such as those for space-based imaging and ophthalmic instrumentation.

3. Design

Each of the actuator electrodes is driven to a certain voltage between 0 and 300V to deflect the mirror in the vicinity of the actuator. The combined effect of all actuators is to impose a well-defined, repeatable contour shape on the mirror surface.

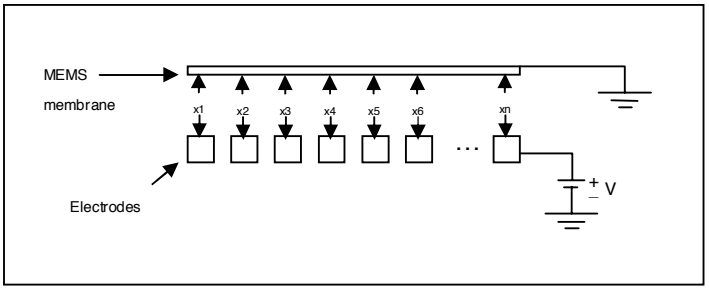

Figure 2 – Single membrane MEMS

The driver chip is divided into segments called that each control one actuator. The driver is designed to form a 12 by 12 array of these segments so that each has an output connected to one electrode, thus charging or discharging them according to an 8-bit digital control signal. Each segment consists of a low voltage and a high voltage circuit. The low voltage circuit manages all low voltage logic and bias inputs while the high voltage circuit converts the low-voltage digital signal into a high voltage analog output.

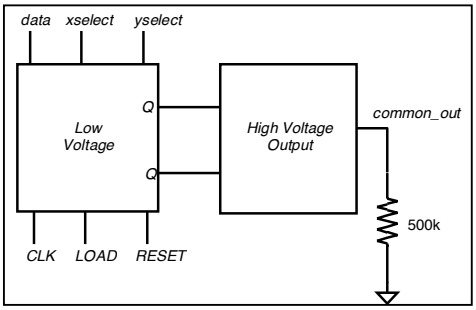

Figure 3 – Single bit

Figure 3 shows a block diagram of a one segment of the circuit to illustrate the concept. The resistor at the output is used to generate the output voltage. The inputs into the low voltage block are summarized below.

Signal	Description
data	8 bit data input
xselect	Output from column decoder
yselect	Output from row decoder
CLK	Global clock signal
LOAD	Synchronous update signal
RESET	Global asynchronous reset signal

The ***LOAD*** signal is the input to allow synchronous update of the entire electrode array. The driver has an option to update the voltage on each electrode as soon as a new data is received or to wait until the entire array is loaded before the outputs are refreshed. The row and column select signals are outputs from decoders which require four bit x and y address inputs.

3.1 Low Voltage Block

The low voltage block consists of a two stage D-latch that uses a single clock signal.

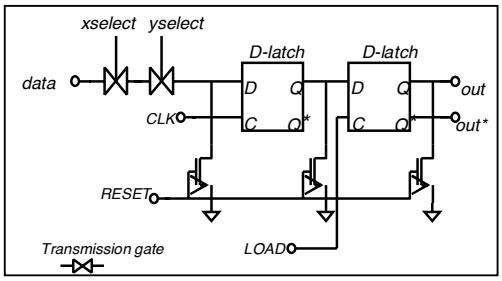

Figure 4 – Low voltage logic

Figure 4 shows the digital logic of one bit. The first latch stores the incoming data input at the rising *CLK* edge, and this bit is not passed onto the second latch until the *LOAD* signal goes high. The output from the second latch is connected into the inputs of the high voltage output stage. The *RESET* signal is independent of the other signals and will reset the outputs of all low voltage logic to ground, thus forcing all the voltage on the electrodes to ground as well.

3.2 High Voltage Block

Since the data stored in the low voltage logic circuit is digital, the output stage must have two functions. One is to perform a digital-to-analog conversion on the 8-bit data signal and the other is to amplify this signal up to 300V. Since high voltage devices are large in physical area, it is necessary to devise a compact circuit that uses minimum number of high voltage transistors.

One of the main challenges encountered in designing the high voltage section is the necessity of a high voltage pass switch. For traditional low voltage circuits, a transmission switch is simple to implement, requiring just two transistors. However in high voltage designs, because the transistor gate cannot withstand the increased voltage, the design is more complicated. There is a need for another method to keep the gate voltage below the breakdown levels whilst passing through a voltage from the source to the drain.

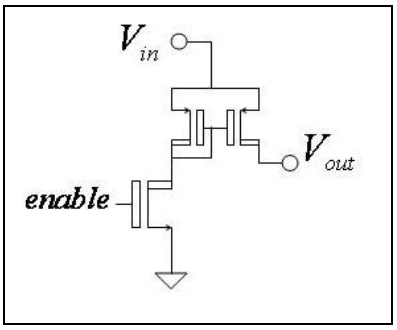

Figure 5 - High voltage switch

Figure 5 shows the implementation of a high voltage switch. The transistors in the current mirror at most see a voltage that is only slightly above its threshold voltage, and then *enable* signal turns the switch on or off. When *enable* is high, V_{in} is passed through

to V_{out}. Although the voltage is fed through, there is current draw from the input port to ground. In normal circumstances when designing a switch this would be undesired, however, in the design of these segments this current draw is used to set the output voltage level. So, with one compact switch design, two problems are solved.

Using this idea, the following circuit was designed.

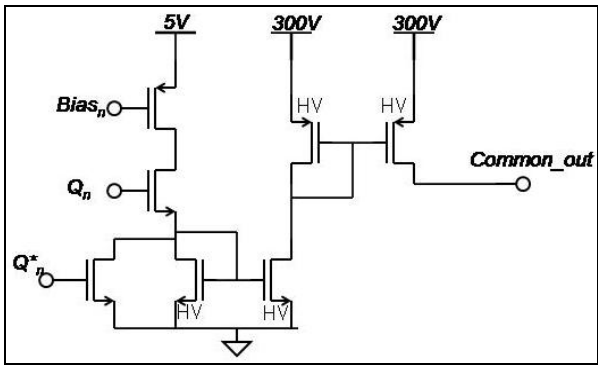

Figure 6 - High voltage output stage

Bias input is signal from a binary weighted current mirror input. The driver has eight bias current inputs each representing a binary bit.

$$\text{i.e.} \qquad I_7 = 2I_6 = 4I_5 = 8I_4 = 16I_3 = 32I_2 = 64I_1 = 128I_0$$

These currents inputs are externally generated, for better tuning ability.

In figure 6, *Qn* are the inputs from the low voltage stage, which switch on or off the bias current to flow down into the high voltage NMOS current mirror, which in turn is mirrored by the high voltage PMOS current mirrors into *Common_out*. This output node from each bit is connected to form a current summing node, and this combined current flows into the 500kΩ resistor shown at the output in figure 3, to generate the output voltage drop.

Thus,

$$common\_out = R_{ref} \sum_{n=0}^{7} b_n I_{bias_n}$$

Where I_{bias_n} are binary weighted bias currents, R_{ref} is the 500kΩ reference resistor and b_n is the input bit.

Based on this relationship, bias currents will have to be tuned so that at maximum input, the output will be 300V.

3.3 Simulation

Low voltage circuits can function at high speeds of up to 1MHz to latch in digital data quickly through the array while the output stages are updating the mirror electrodes at a

slower rate. This is an advantage of the two latch stage design. The individual output stages only need to function at 100Hz, which is the response rate of the MEMS structure.

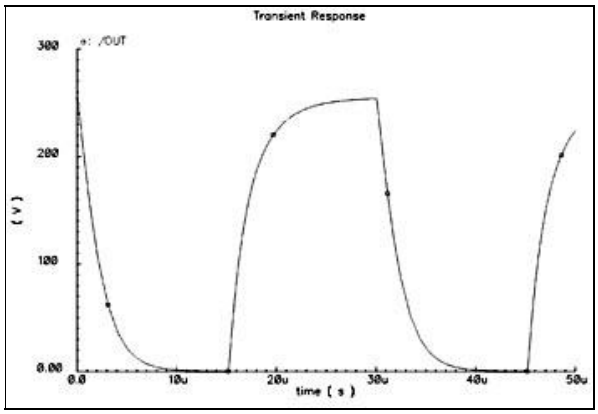

Figure 7 - Simulated output

Figure 7 shows the simulated output from one pixel. The input bias currents are set such that at maximum input data, the output is 255V, as shown. Since these bias currents are used to charge the electrodes, lower currents will lead to slower charging times. Figure 7 is shown with the least significant bias current at 1μA.

3. Layout and Fabrication

Even with the advances in integrated circuit fabrication technology, an operating voltage of 300V is not common. Thus, it was important to choose a foundry that can fabricate devices that function at this high voltage but also have the capability of building low voltage devices on the same substrate. We chose DALSA semiconductors for their wide variety of devices and the option for high-resistive poly layer, which helps in making the layout compact since a physically smaller resistor is sufficient.

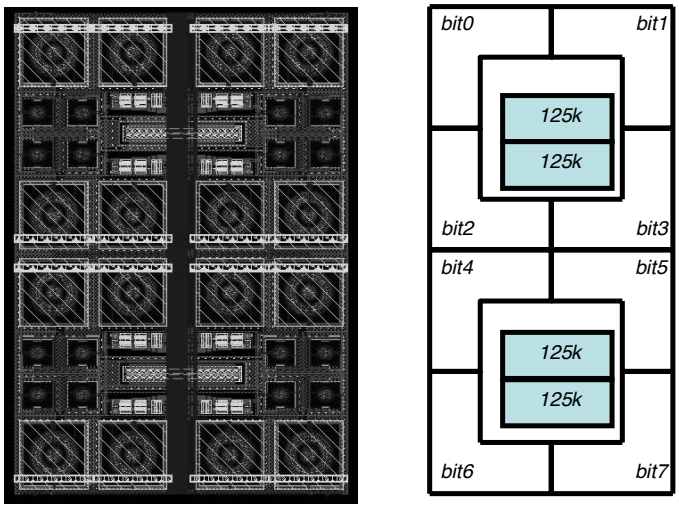

Figure 7a,b – Layout and overview of one pixel

Figure 7 shows the layout of one pixel, which measures 957μm wide and 1370μm high. As it can be seen, high voltage devices occupy a much larger area thus the need for a compact high voltage output stage. The 500kΩ output resistor is divided into four 125kΩ resistors for improved area use. These resistors lay above a biased n-doped well in order to prevent oxide breakdown. They are made up of lightly doped, highly resistive polysilicon and are not rated to withstand 300V. So after collaborating with the foundry engineers, the resistors were put above a well that was biased at 100V.

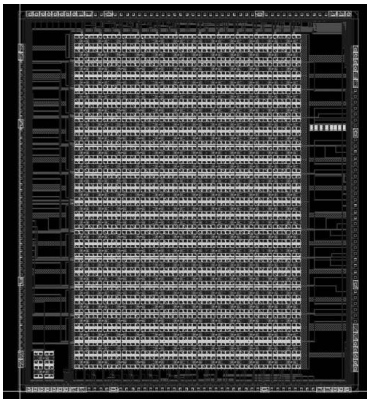

Figure 8 – Chip layout

Figure 8 shows the layout of the entire chip, whose physical size is 17mm wide by 19mm high. This is the maximum allowed size of a die site by the foundry, and it was important to keep the layout as compact as possible to keep inside this area. The small pixel in the corner is a tuner cell used to tune the bias currents that are used to generate the binary weighted output.

Figure 9 shows the actual fabricated chip.

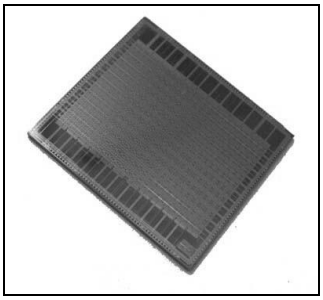

Figure 9 - Fabricated driver chip

4. Testing

Because of the large die size of the chip, it was not possible to buy pre-manufactured packages with a cavity that can fit it. Since obtaining a custom made package is

expensive, it was decided to build a prototype test structure that could be used to verify the functionality of the chip before a custom package was ordered.

We have built a test bed where we use two PCB's (printed-circuit-boards), one as a chip carrier and the other as a test board. The number of input/outputs were limited to twenty on each side by bonding just four outputs, thereby simplifying testing, and bonding.

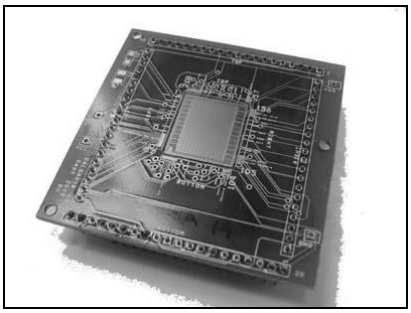

Figure 10 - Chip carrier PCB

Figure 10 shows the smaller PCB that houses the driver chip. The PCB has a cut-out in the center where the chip is attached down onto a copper plate, which also serves as a small heat sink. This PCB has eighty pins that extend vertically down to allow it to be plugged into a test PCB that holds the test setup.

Figure 11 shows the test PCB.

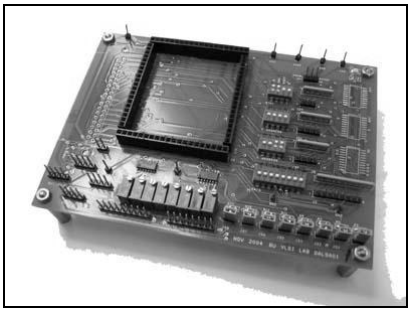

Figure 11 - Test PCB

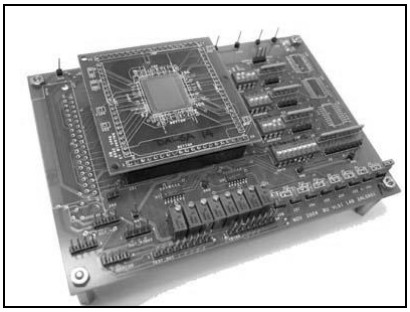

Figure12 – Complete test setup

Figure 12 shows the carrier PCB plugged into the test PCB. The eight current sources can be tuned using the potentiometers on the bottom of the PCB and the digital inputs can be set using the switches on the right. Four outputs from each side are measured from the output headers on the bottom left.

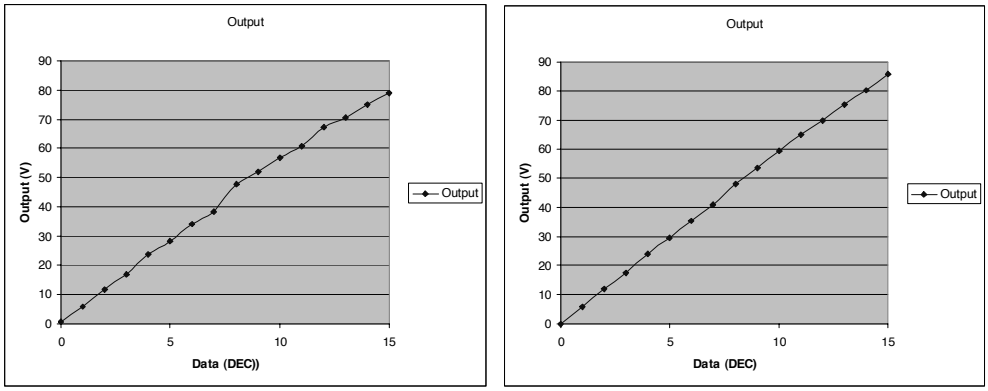

Figure 1 – Roughly tuned and correctly tuned output at 90V

Figure 5 shows one of the outputs from the test setup. The first graph shows a roughly tuned output which can be individually fine tuned to achieve a linear monotonic response. The driver chip was tested at up to 200V supply voltage, which was the maximum voltage the test setup can handle.

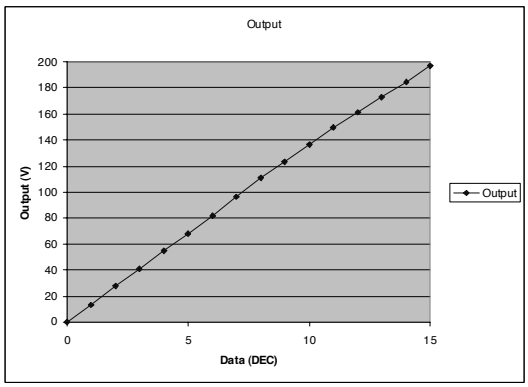

Figure 2 - Output at 200V

Figure 6 shows the output at 200V, which also shows a precise linear response.

The above results are when the driver functions as designed. However it was observed that sometimes the outputs of the driver are latched at the highest supply voltage rail and does not adjust with the changing input data. It is believed this is due to some voltage coupling from high voltage lines onto low voltage gates that have low threshold voltages. These induced voltages could be switching on some low voltage transistors and causing the latch-up effect.

5. Acknowledgements

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